REMARKS

Claims 1 and 3-9 are pending in this application, of which claim 1 is independent. In this Amendment, claim 1 has been amended. Care has been exercised to avoid the introduction of new matter. Support for the amendments to the claim can be found on, for example, page 7, lines 13-16; and page 8, lines 12-15 of the specification.

Information Disclosure Statement

The Office Action dated May 3, 2006, has acknowledged the submission of the Information Disclosure Statement of April 12, 2004, and stated that the cited references have been considered. It is noted, however, that the form PTO-1449 exhibits the Examiner's initials for only two of the three references that were submitted and listed on the form, presumably an inadvertent error. Acknowledgement of consideration of the AMBA publication in a further copy of the PTO-1449 is respectfully solicited for clarification of the record.

Claim Rejections—35 U.S.C. § 102

Claims 1 and 3-8 have been rejected under 35 U.S.C. § 102(b) as being unpatentable over Ganapathy et al. Applicant submits that Ganapathy et al. does not identically disclose a direct memory access controller including all the limitations recited in independent claim 1. Specifically, the reference does not disclose, among other things, the following limitations recited in claim 1 (emphasis added):

> two groups of registers including a first group for current transfer and a second group for next transfer which is different from said first group for current transfer and includes device information representing a device from which a data transfer

request is accepted, values set in two groups being for controlling the direct memory access transfer,

wherein said control portion permits transferring to a first portion of said direct memory access transfer portions based on values set in said first group, and permits transferring to a second portion of said direct memory access transfer portions based on values set in said second group after transferring by said first portion when the control portion receives the data transfer request from the device represented by the device information, in one granting period of transferring by the arbiter.

The direct memory access controller is coupled with the arbiter which arbitrates the bus right between the direct memory access controller and another circuit, for example, the central processing unit. The direct memory access controller includes plural direct memory access transfer portions (plural channels), the control portion, and the two groups of registers. The second group of the registers includes a register having a device information representing a device from which a data transfer request is accepted. The control portion permits one of the plural direct memory access transfer portions based on the second group of registers when the control portion receives the data transfer request from the device represented by the device information, in the granted period of the arbiter.

Ganapathy et al. discloses a distributed direct memory access method. DMA controller units are distributed to various functional modules desiring direct memory access. A bus multiplexes a number of DMA transactions at one time, and one transaction of the DMA is dealt at a time. Accordingly, Ganapathy does not disclose the direct memory access controller, which performs plural data transfer transactions in one granting period by the bus arbiter. Furthermore, Applicant emphasizes that Ganapathy does not disclose device information in the second group for the next DMA transactions, and also does not disclose that the DMA transaction is started by receiving the data transfer request from the device represented by the device information.

In contrast, the claimed second group for next transfer includes device information representing a device from which a data transfer request is accepted, and the claimed control portion permits transferring to a second portion of the direct memory access transfer portions based on values set in the second group after transferring by the first portion when the control portion receives the data transfer request from the device represented by the device information, in one granting period of transferring by the arbiter.

Based on the foregoing, Applicant submits that Ganapathy et al. does not identically disclose a direct memory access controller including all the limitations recited in independent claim 1. Dependent claims 3-8 are also patentably distinguishable over Ganapathy et al. at least because these claims respectively include all the limitations recited in independent claim 1. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claims and favorable consideration thereof.

Claim Rejections—35 U.S.C. § 103

Claim 9 has been rejected under 35 U.S.C. § 103(a) as being unpatentable over Ganapathy et al. in view of Levenstein. This rejection is respectively traversed.

Claim 9 depends on independent claim 1. Applicant thus incorporates herein the arguments made in response to the rejection of the independent claim 1 under 35 U.S.C. § 102 for anticipation evidenced by Ganapathy et al. The Examiner's additional comments and secondary reference to Levenstein do not cure deficiencies of Ganapathy et al. Applicant, therefore, respectfully solicits withdrawal of the rejection of the claim and favorable consideration thereof.

Conclusion

It should, therefore, be apparent that the imposed rejections have been overcome and that all pending claims are in condition for immediate allowance. Favorable consideration is, therefore, respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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